

10001421  
11/02/01

PATENT NUMBER and  
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU
10001421	11/02/2001	22857	738	1725

EXAMINER  
S. JONER-K  
H. W.

\*\*APPLICANTS: Milewski Joseph; Woychik Charles;

\*\*CONTINUING DATA VERIFIED:

THIS APPLICATION IS A DIV OF 08/815,656 03/13/1997 PAT 6,330,967

\*\* FOREIGN APPLICATIONS VERIFIED:

PG-PUB	DO NOT PUBLISH <input checked="" type="checkbox"/>	RESCIND <input type="checkbox"/>	
Foreign priority claimed	<input type="checkbox"/> yes <input checked="" type="checkbox"/> no	ATTORNEY DOCKET NO	
35 USC 113 conditions met	<input type="checkbox"/> yes <input checked="" type="checkbox"/> no	END919970013US2	
Verified and Acknowledged Examiner's initials <i>JW</i>			
TITLE : Low temperature solder chip attach structure		U.S. DEPT. OF COMM./PAT. & TM-PTO-436 (Rev. 12-91)	

NOTICE OF ALLOWANCE MAILED

ISSUE FEE

Amount Due  Date Paid

TERMINAL

DISCLAIMER

Assistant Examiner

Primary Examiner

PREPARED FOR ISSUE

CLAIMS ALLOWED

Total Claims

Print Claim for  
0.0

DRAWING

Sheets Drawn

Figs Drawn

Print Fig.

Application Examiner

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ISK (CRF)

CD-ROM

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